

Docket No.: 43876-154

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of	:	Customer Number: 20277
	:	
Craig HANSEN et al	:	Confirmation Number: To be assigned
	:	
Serial No.: Unknown	:	Art Unit: To be assigned
Continuation of	:	
Application No. 10/646,787	:	
Filed: August 25, 2003	:	
	:	
Filed: January 15, 2004	:	Examiner: To be assigned
	:	
For:		<b>METHOD AND SOFTWARE FOR MULTITHREADED PROCESSOR WITH PARTITIONED OPERATIONS</b>

**SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Mail Stop NEW APPLICATIONS  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Continuation of  
Application No. 10/646,787  
Filed August 25, 2003

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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**Date: January 15, 2004**

WDC99 866165-1.043876.0154

<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <b>(PTO-1449)</b>				ATTY. DOCKET NO. <b>43876-154</b>		SERIAL NO. <b>Continuation of Serial No. 10/646,787</b>	
				APPLICANT <b>Craig HANSEN et al</b>			
				FILING DATE <b>Jan. 15, 2004</b>		GROUP <b>To be assigned</b>	
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		US 5,819,101	10/6/1998	Alexander Peleg, et al			
		US 5,881,275	3/9/1999	Alexander Peleg, et al			
		US 6,119,216	9/12/2000	Alexander Peleg, et al			
		US 6,516,406	2/4/2003	Alexander Peleg, et al			
		US 6,539,467	3/25/2003	Timothy D. Anderson, et al			
		US 6,574,724	6/3/2003	David Hoyle, et al			
		US 6,631,389 B2	10/7/2003	Derrick Chu Lin, et al			
		US					
		US					
		US					
		US					
<b>FOREIGN PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
EXAMINER				DATE CONSIDERED			

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

WDC99 866167-1.043876.0154

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		US 4,785,393	11/15/1988	Chu et al.			
		US 4,814,976	03/21/1989	Craig C. Hansen, et al.			
		US 5,031,135	07/09/1991	Patel			
		US 5,280,598	01/1994	Osaki et al.			
		US 5,481,686	01/02/1996	Dockser			
		US 5,487,024	01/1996	Girardeau Jr.			
		US 5,600,814	02/1997	Gahan et al.			
		US 5,740,093	04/14/1998	Sharangpani			
		US 5,742,840	04/21/1998	Hansen et al.			
		US 5,768,546	06/1998	Kwon			
		US 5,898,849	04/27/1999	Tran			
		US 5,996,057	11/30/1999	Hunter L. Scales, III, et al.			
		US 6,041,404	03/21/2000	Patrice Roussel, et al.			
		US 6,052,769	04/18/2000	Thomas R. Huff, et al.			
		US 6,173,393 B1	01/09/2001	Salvador Palanca, et al.			
		US 6,275,834 B1	08/14/2001	Derrick Chu Lin, et al.			
		US 6,295,599	09/2001	Hansen et al.			
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		IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications And Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (March 1992)					
		IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995)					
		IBM, "The PowerPC Architecture: A Specification For A New Family of Risc Processors", 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994).					
		Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set", Manual Part No. 09740-90039, (1990).					
		MIPS Computer Systems, Inc., "MIPS R4000 User's Manual", Mfg. Part No. M8-00040, (1990).					
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Continuation of Application No. 10/646,787  
Filed August 25, 2003  
Docket: 43876-154

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 10/646,787 , filed August 25, 2003 , which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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Registration No. 44,489

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**Date: January 15, 2004**

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				FILING DATE <b>January 15, 2004</b>		GROUP <b>To be assigned</b>	
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
	4,025,772	05/24/77	Constant				
	4,489,393	12/18/84	Kawahara, et al.				
	4,701,875	10/20/87	Konishi, et al.				
	4,727,505	02/23/88	Konishi, et al.				
	4,876,660	10/24/89	Owens, et al.				
	4,893,267	01/09/90	Alsup, et al.				
	4,956,801	09/11/90	Priem et al.				
	4,969,118	11/06/90	Montoye, et al.				
	4,975,868	12/04/90	Freerksen				
	5,032,865	07/16/91	Schlunt				
	5,157,388	10/20/92	Kohn				
	5,201,056	04/06/93	Daniel, et al.				
	5,268,855	12/07/93	Mason, et al.				
	5,268,995	12/07/93	Diefendorff, et al.				
<b>FOREIGN PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
	Parallel Computers for Graphics Applications, Adam Levinthal, Pat Hanrahan, Mike Paquette, Jim Lawson, Pixar San Rafael, California, 1987						
	Organization of the Motorola 88110 Superscalar RISC Microprocessor, Keith Diefendorff and Michael Allen; IEEE Micro., April 1992, 40-63						
	Microprocessor Report, Volume 7 Number 13, October 4, 1993, IBM Regains Performance Lead with Power2, Six Way Superscalar CPU in MCM Achieves 126 SPECint92.						
	IBM Creates PowerPC Processors for AS/400, Two New CPU's Implement 64-Bit Power PC with Extensions by Linley Gwennap, July 31, 1995, 15-16						
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EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
	5,408,581	04/18/95	Suzuki, et al.				
	5,423,051	06/06/95	Fuller, et al.				
	5,426,600	06/20/95	Nakagawa, et al.				
	5,500,811	03/19/96	Corry				
	5,557,724	09/17/96	Sampat, et al.				
	5,588,152	12/24/96	Dapp, et al.				
	5,592,405	01/07/97	Gove, et al.				
	5,640,543	06/17/97	Farrell, et al.				
	5,642,306	06/24/97	Mennemeier, et al.				
	5,666,298	09/09/97	Peleg, et al.				
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	5,673,407	09/30/97	Poland, et al.				
	5,675,526	10/07/97	Peleg, et al.				
	5,680,338	10/21/97	Agarwal, et al.				
<b>FOREIGN PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
	0 474 246 A2	06/09/91	Europe				
	0 654 733 A1	05/07/94	Europe				
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
	The Visual Instruction Set (VIS) in UltraSPAR <sup>TM</sup> , L. Kohn, G. Maturana, M. Tremblay, A. Prabhu, G. Zyner, May 3, 1995, 462-469						
	Osborne McGraw-Hill, i860 <sup>TM</sup> Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn, 1990, 8-10; 171-175, 182-183						
	A General-Purpose Array Processor for Seismic Processing, Nov-Dec., 1984, Volume 1, No. 3) Revisiting past digital signal processor technology, Don Shaver- Jan-Mar. 1998. 5-26						
	Accelerating Multimedia with Enhanced Microprocessors, Ruby B. Lee, 1995.						
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EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
	5,721,892	02/24/98	Peleg, et al.				
	5,734,874	03/31/98	Van Hook, et al.				
	5,757,432	05/26/98	Dulong, et al.				
	5,758,176	05/26/98	Agarwal, et al.				
	5,802,336	09/01/98	Peleg, et al.				
	5,809,292	09/15/98	Wilkinson, et al.				
	5,818,739	10/06/98	Peleg, et al.				
	5,825,677	10/20/98	Agarwal, et al.				
	5,835,782	11/10/98	Chu Lin, et al.				
	5,886,732	03/23/99	Humpleman				
	5,922,066	07/13/99	Cho, et al.				
	5,983,257	11/09/99	Dulong, et al.				
	6,016,538	01/18/00	Guttag, et al.				
	6,092,094	07/18/00	Ireton				
	6,401,194 B1	06/04/02	Nguyen, et al.				
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